Motherboard Pin	Name	Direction	Description
1	/IOSEL	→	I/O Select. Active when page $Cn gets accessed. N.C. on slot 0
2	A0	↔	Buffered address bus
3	A1	↔	Buffered address bus
4	A2	↔	Buffered address bus
5	A3	↔	Buffered address bus
6	A4	↔	Buffered address bus
7	A5	↔	Buffered address bus
8	A6	↔	Buffered address bus
9	A7	↔	Buffered address bus
10	A8	↔	Buffered address bus
11	A9	↔	Buffered address bus
12	A10	↔	Buffered address bus
13	A11	↔	Buffered address bus
14	A12	↔	Buffered address bus
15	A13	↔	Buffered address bus
16	A14	↔	Buffered address bus
17	A15	↔	Buffered address bus
18	R/W	↔	Buffered Read/Write signal.
19	SYNC	→	Only Slot 7. SYNC from Video Generator. Not on Rev 0 Boards. Testpin on Slot 1 for //e
20	/IOSTRB	→	I/O Strobe. Active when $C800 and $CFFF gets accessed
21	/RDY	←	Activation during Phi1 will halt the CPU, with the address bus holding the last address
22	/DMA	←	Activation disables the 6502"s address bus and halts the CPU
23	/INTOUT	←	Daisy-chained interrupt output to lower priority devices
24	/DMAOUT	←	Daisy-chained DMA output to lower priority devices
25	+5V	—	+5 Volt power supply. Max. 500mA for ALL peripheral boards
26	GND	—	System electrical ground
27	/DMAIN	→	Daisy-chained DMA input from higher priority devices
28	/INTIN	→	Daisy-chained interrupt input from higher priority devices
29	/NMI	←	Non-Maskable Interrupt. Monitor ROM starts interrupt handling routine at location $3FB
30	/IRQ	←	Interrupt ReQuest. Monitor starts the routine pointed to by $3FE/F
31	/RES	←	RESet
32	/INH	←	INHibits the on board ROMs ($D000-$FFFF)
33	-12V	—	-12 Volt power supply. Max. 200mA for ALL peripheral boards
34	-5V	—	-5 Volt power supply. Max. 200mA for ALL peripheral boards
35	COLORREF	→	Only Slot 7. 3.5 MHz Video COLOR REF. Not on Rev 0 Boards. Testpin on Slot 1 for //e. M2B0 on A2gs
36	7M	→	7Mhz clock

37	Q3	→	2Mhz asymetrical clock
38	PHI1	→	1 MHz phase 1 clock
39	Various	→	USER1 on A2: Disable adressdecode. 65C02 SYNC on A2e. M2SEL on A2gs
40	PHI0	→	1 MHz phase 0 clock (Inverted PHI1)
41	/DEVSEL	→	DEVice SELect. Active when $C0nX gets accessed; n - Slot#+8
42	D7	↔	Buffered bi-directional data bus
43	D6	↔	Buffered bi-directional data bus
44	D5	↔	Buffered bi-directional data bus
45	D4	↔	Buffered bi-directional data bus
46	D3	↔	Buffered bi-directional data bus
47	D2	↔	Buffered bi-directional data bus
48	D1	↔	Buffered bi-directional data bus
49	D0	↔	Buffered bi-directional data bus
50	+12V	-?-	+12 Volt power supply. Max. 250mA for ALL peripheral boards