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# Pinouts

Navigaton History:
Pinouts

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Disclaimer: These haven't been verified these, but they did appear to be posted by reliable people.

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## Apple II+ / IIe / Stealth IIgs Power Connector

```
Power Supply Connector Socket      Power Supply Output Ratings

         _________
        /         \                +5V @ 2.50 Amps (continuous)
   -12V |  5   6  |   -5V          -5V @ 0.25 Amps (continuous)
        |         |               +12V @ 1.50 Amps (continuous)
    +5V |  3   4  |  +12V         -12V @ 0.25 Amps (continuous)
        |         |
    GND |  1   2  |   GND
        |_________|
```

- = Denotes IIgs ROM 00/01 with installed connector as in Stealth IIgs or Service Stock IIgs Motherboards (so they could be used in either Stealth or standard IIgs cases) This also applies for the 26 pin keyboard connector.

## GS Motherboard Power Connector

```
 _
|_|
|7|  -5V             0.25 A
|6| -12V             0.25 A
|5| +12V             1.0 A
|4|  +5V             4.0 A
|3|  N/C - KEY
|2|  GND
|1|  GND
|_|
```

The pins are numbered as above when you are sitting in front of the computer, i.e. 7 is closest to the back of the motherboard.

## Apple Game Port (9-pin Connector)

```
   ,--------------------.
   \  5   4   3   2   1  /
    \   9   8   7   6   /
     `-----------------'

Pin 1 - Pushbutton 1
Pin 2 - +5V Power
Pin 3 - Ground
Pin 4 - Game Control 2 or PDL2 (Joystick-2 X-axis)*
Pin 5 - Game Control 0 or PDL0 (Joystick-1 X-axis)
Pin 6 - Pushbutton 2*
Pin 7 - Pushbutton 0 (usually the "Fire" button)
Pin 8 - Game Control 1 or PDL1 (Joystick-1 Y-axis)
Pin 9 - Game Control 3 or PDL3 (Joystick-2 Y-axis)*
```

- Note: These functions are not available on the //c or IIc+.

## Apple 16-Pin DIP Socket (Internal)

All Apple II / Compatibles with slots have this connector internally.

```
                              =========
```

```
  Pushbutton 3 (GS only)  9 | *     * | 8  Ground
   Gm Ctrl 1 (Stick-1 Y) 10 | *     * | 7  Gm Ctrl 2 (Stick-2 X)
   Gm Ctrl 3 (Stick-2 Y) 11 | *     * | 6  Gm Ctrl 0 (Stick-1 X)
          Annunciator 3  12 | *     * | 5  /$C040 Strobe (][,][+,IIe only, +5V pullup o
          Annunciator 2  13 | *     * | 4  Pushbutton 2
          Annunciator 1  14 | *     * | 3  Pushbutton 1
          Annunciator 0  15 | *     * | 2  Pushbutton 0
          No Connection  16 | *     * | 1  +5V
                            ===| |===
                               ^
                          Notch on socket
                   (faces toward front of computer)
```

Game Port Information (with BASIC Peek/Poke locations) obtained from pages 430-433 of the Apple // User's Guide, Second Edition by Lon Poole:

-16296 Annunciator 0 Off

Turns off game control output (annunciator) number 0. The voltage on pin 15 of the game control is set to approximately 0 volts (TTL low).

-16295 Annunciator 0 On

Turns on game control output (annunciator) number 0. The voltage on pin 15 of the game control is set to approximately +5 volts (TTL high).

The following annunciator soft switches follow the same rules as annunciator 0 for their respective pin assignments:

-16294 Annunciator 1 Off -16293 Annunciator 1 On

-16292 Annunciator 2 Off -16291 Annunciator 2 On

-16290 Annunciator 3 Off -16289 Annunciator 3 On

-16287 Read Pushbutton 0

When the pushbutton on game control number 0 or the open-apple key is being pressed, the value in this location exceeds 127. When it is not being pressed, the value is 127 or less.

The following pushbutton soft switches follow the same rules as pushbutton 0 for their respective pin assignments:

-16286 Read Pushbutton 1

-16285 Read Pushbutton 2

-16272 Stobe Output

Normally pin 5 of the game control connector is +5 volts. If you PEEK memory location -16285, it drops to 0 volts for one-half microsecond. POKE will trigger the strobe twice.

The following is a direct exerpt from page 167 of the Apple //e Reference Manual:

"The hand-control inputs are connected to the timing inputs of an NE558 quadruple 555-type analog timer. Addressing $C07x sends a signal from the 74LS154 that resets all four timers and causes their outputs to go one (high). A variable resistance of up to 150K ohms connected between one of these inputs and the +5V supply controls the charging time of one of four 0.022-microfarad capacitors. When the voltage on the capacitor passes a certain threshhold, the output of the NE558 changes back to zero (low).

Programs can determine the setting of a variable resistor by resetting the timers and then counting time until the selected timer input changes from high to low. The resulting count is proportional to the resistance."

Basically, the above excerpt is a long description of the BASIC PDL() function.

## Apple //e Expansion (Peripheral) slot

The following is a direct excerpt from pages 172-174 of the Apple //e Reference Manual regarding the pin-out of the expansion slots:

Pin 1 – I/0 SELECT – Normally high; goes low during phase 0 when the 6502 addresses location $CnXX, where n is the connector number. This line can drive 10 LS TTL loads.*

Pin 2-17 – AO-A15 – Three-state address bus. The address becomes valid during phase 1 and remains valid during phase 0. Each address line can drive 5 LS TTL loads.*

Pin 18 – R/W' – Three-state read/write line. Valid at the same time as the address bus; high during a read cycle, low during a write cycle. It can drive 2 LS TTL loads.*

Pin 19 – SYNC' – Composite horizontal and vertical sync, on expansion slot 7 ONLY. This line can drive 2 LS TTL loads.*

Pin 20 – 1/0 STROBE' – Normally high; goes low during phase 0 when the 6502 addresses a location between Sc800 and $CFFF. This line can drive 4 LS TTL loads.*

Pin 21 – RDY – Input to the 6502. Pulling this line low during phase 1 halts the 6502 with the address bus holding the address of the location currently being fetched. This line has a 3300 ohm pullup resistor to +5V.

Pin 22 – DMA' – Input to the address bus buffers. Pulling this line low during phase 1 disconnects the 6502 from the address bus. This line has a 3300 ohm pullup resistor to +5V.

Pin 23 – INT OUT – Interrupt priority daisy-chain output. Usually connected to pin 28 (INT IN). Note: On slot 7 ONLY, this pin can be connected to the graphics-mode signal GR (Not available on revision A boards).

Pin 24 – DMA OUT – DMA priority daisy-chain output. Usually connected to pin 22 (DMA IN).

Pin 25 – +5V – +5V power supply. A total of 500' is available for all accessory cards.

Pin 26 – GND – System common ground.

Pin 27 – DNA IN – DMA priority daisy-chain input. Usually connected to pin 24 (DMA OUT).

Pin 28 – INT IN – Interrupt priority daisy-chain input. Usually connected to pin 23 (INT OUT).

Pin 29 – NMI' – Non-maskable interrupt to 6502. Pulling this line low starts an interrupt cycle with the interrupt-handling routine at location $03FB. This line has a 3300 ohm pullup resistor to +5V.

Pin 30 – IRQ' – Interrupt request to 6502. Pulling this line low starts an interrupt cycle only if the interrupt-disable (I) flag in the 6502 is not set. Uses the interrupt-handling routine at location $03FE. This line has a 3300 ohm pullup resistor to +5V.

Pin 31 – RES' – Pulling this line low initiates a reset routine.

Pin 32 – INH' – Pulling this line low during phase 1 inhibits (disables) the memory on the main circuit board. This line has a 3300 ohm pullup resistor to +5V.

Pin 33 – -12V – -12V power supply. A total of 200mA is available for all accessory cards.

Pin 34 – -5V – -5V power supply. A total of 200mA is available for all accessory cards.

Pin 35 – 3.58M – 3.58MHz color reference signal, on slot 7 ONLY. This line can drive 2 LS TTL loads.*

Pin 36 – 7M – System 7MHz clock. This line can drive 2 LS TTL loads.*

Pin 37 – Q3 – System 2MHz asymmetrical clock, This line can drive 2 LS TTL loads.*

Pin 38 – PHASE1 – 6502 phase 1 clock. This line can drive 2 LS TTL loads.*

Pin 39 – uPSYNC – The 6502 signals an operand fetch by driving this line high during the first read cycle of each instruction.

Pin 40 – PHASEO – 6502 phase 0 clock. This line can drive 2 LS TTL loads.*

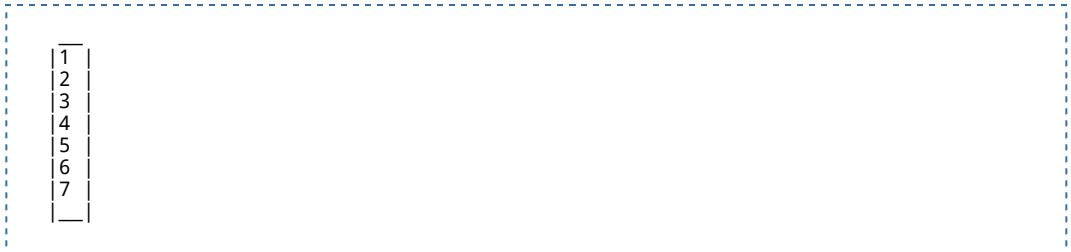
Pin 41 – DEVICE SELECT' – Normally high; goes low during phase 0 then the 6502 addresses location $C0nX, where n is the connector number plus 8. This line can drive 10 LS TTL loads.*

Pin 42-49 – D0-D7 – Three-state buffered bi-directional data bus. Data becomes valid during phase 0 high and remains valid until phase 0 goes low. Each data line can drive one LS TTL load.*

Pin 50 – +12V – +12V power supply. A total of 250mA is available for all accessory cards.

- Loading limits are for each card.

## Apple IIc Plus Internal Modem Connector



```
Pin  Signal  Description

1    -5V     -5 Volts
2    RXD     Receive Data
3    TXD     Transmit Data
4    DCD     Data Carrier Detect
5    DTR     Data Terminal Ready
6    DSR     Data Signal Ready
7    GND     Ground
```

## Mini DIN-8 Serial Port (GS, IIc Plus, Macintosh)

[and pinouts to connect to a serial DB-25 printer]

The IIgs serial port is numbered as follows, looking at the back of the computer:

```
8 7 6
5 4 3
 2 1

The wiring for a serial printer cable (==modem cable) would be as follows:

IIgs                Printer (DB-25)

1  Hshk Out   -----  6 DSR  (or possibly 5 CTS, or 8 DCD)
2  HShk In    -----  20 DTR (or possibly 4 RTS)
3  TxD        -----  3 RxD
4  Gnd        -----  7 Signal Ground
5  RxD        -----  2 TxD
6  TxD+  No connection
7  GPI   No connection
8  RxD+  Loop to signal ground (pin 4 at IIgs or pin 7 at printer)
```

(Cable shield should be connected to shielding at the IIgs end, and to pin 1 at the printer end.)

By comparison, a modem cable will swap pins 1 and 2, and pins 3 and 5 (using the numbering of the IIgs end).

## //c (5-pin) Serial Port, Null Modem Cable

```
5       1
 4     2
    3

The functions are:

1  Handshake Out (nominally DTR)
2  Data Out (TxD)
3  Ground
4  Data In (RxD)
5  Handshake In (nominally DSR)

<pre>

To wire up a IIc to a simple modem without hardware handshaking, use the following pi

<pre>

IIc     Modem
DIN-5   DB-25M
1 ----- 20 DTR
2 ----- 2  TxD
3 ----- 7  Gnd
4 ----- 3  RxD
5 ----- 6  DSR   (you might want to use pin 8, DCD in some cases)
```

The IIc cannot do hardware handshaking very well, but this is as close as you can get:

```
IIc     Modem
DIN-5   DB-25M

1 ----- 4  RTS
2 ----- 2  TxD
3 ----- 7  Gnd
4 ----- 3  RxD
5 ----- 5  CTS
```

The IIc's handshaking lines have annoying side effects, which cause problems with hardware handshaking.

1. The "Handshake Out" signal is implemented to mean "I want to send data" (the official and original meaning of RTS). If you turn off the output handshake line, the IIc will stop sending data. For a hardware handshaking modem, RTS is supposed to mean "You are allowed to send me data" (from the computer's point of view).

If the computer tells the modem to stop transmitting, the computer

will also be unable to transmit. This will reduce the rate at which data can be transferred bidirectionally, but doesn't cause any other problems.

2. The "Handshake In" signal is implemented to mean "There is receive data present" (the official meaning of DCD). tf the incoming handshake line is disabled, the IIc will stop receiving data (ignore any data on RxD). For a hardware handshaking modem, CTS is supposed to mean "You are allowed to send me data" (from the modem's point of view).

If the modem tells the computer to stop transmitting, the computer will also be unable to receive, and will discard any data sent by the modem while CTS is not active. This can cause screen corruption and loss of data blocks or acknowledgements during a file transfer, which will require retransmission. It is only likely to be a problem while a lot of data is being sent, so is more likely to cause problems during a file upload than a download.

If the comms software is quick enough, it can drop RTS immediately when CTS is lowered, which will prevent the modem from sending any more data.

You will need the //c System Utilities disk to set up the serial port speeds, or a comm program that overrides them anyway.

Max speed is 9600.

## Non-Apple DE9 and DB25 Serial Ports

Pinouts are for looking at the back of the computer, as usual.

```
DB-25
,-------------------------------------------------.
\ 13  12  11  10  09  08  07  06  05  04  03  02  01 /
 \  25  24  23  22  21  20  19  18  17  16  15  14  /
  `-----------------------------------------------'

DE-9
,-------------------.
\ 5   4   3   2   1 /
 \  9   8   7   6  /
  `---------------'

pin#  DB-25     DE-9
----  ------   ------
shield  gnd     gnd
    1   gnd     DCD
    2   TD      RD
    3   RD      TD
    4   RTS     DTR
    5   CTS     SG
    6   DSR     DSR
    7   SG      RTS
    B   DCD     CTS
    9   +dcv    RI
   10   -dcv (DC test voltage) [DCE->DTE]
   11   QM
   12   (S)DCD
   13   (S)CTS
   14   (S)TD, NS, [fault on IW1]
   15   TC [DCE->DTE]
   16   (S)RD, DCT
```

```
    17   RC
    18   DCR
    19   (S)RTS
    20   DTR
    21   SQ
    22   RI
    23   data rate selector
    24   (TC) [DTE->DCE]
    25   busy
```

## IIGS (and Apple ///) RGB Connector

```
pin #           signal
 1              ground (for red 'P)
 2              red
 3              composite sync. (in German: Farbmischsynchronisation)
 4              not used
 5              green
 6              ground (for gzeen ¿)
 7              -5 V
 8              +12 V
 9              blue
10              not used
11              audio output (not used)
12              monochrome screen off (???)
13              ground (for blue ?)
14              not used
15              not used
                system ground
                   |
          ,--------|-------------------------.
         \ 8    7    6    5    4    3    2    1 /
          \  15   14   13   12  11   10    9   /
           `---------------------------------'
```

## 6502/65C02 Pinouts

> Does anyone know what each of the pins on the 6502 CPU chip in the Apple > II Plus does?

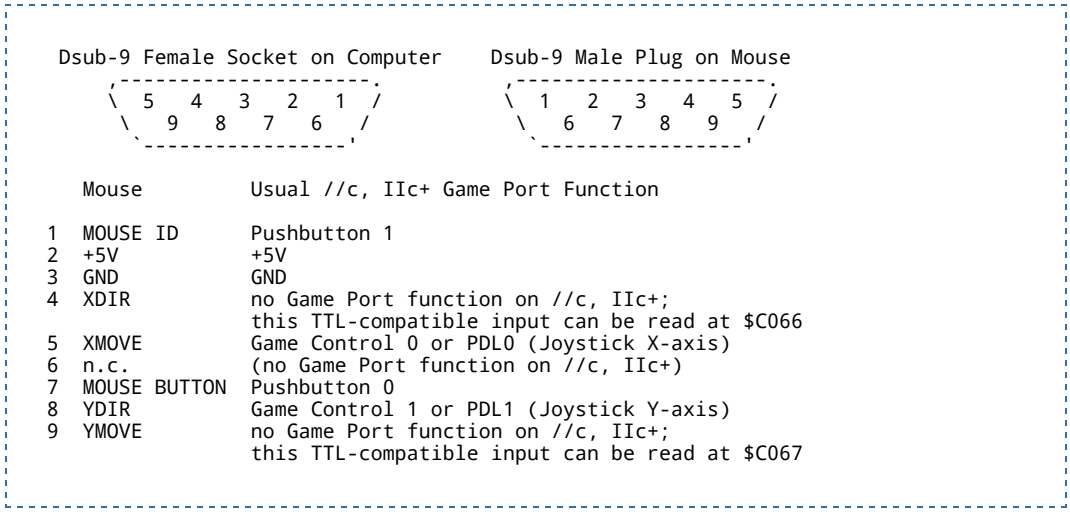
They all plug into the socket on the motherboard to keep the chip from drifting away.

```
          Vss 1   |_|  40 ~RESET
          RDY 2        39 Phase 2 OUT
Phase 1 OUT 3        38 SO
       ~IRQ 4        37 Phase 0 IN
       (NC) 5        36 (NC)
       ~NMI 6        35 (NC)
       SYNC 7        34 R/~W
        Vcc 8        33 D0
       A0   9        32 D1
       A1  10        31 D2
       A2  11        30 D3
       A3  12        29 D4
       A4  13        28 D5
       A5  14        27 D6
       A6  15        26 D7
       A7  16        25 A15
       A8  17        24 A14
       A9  18        23 A13
       A10 19        22 A12
       A11 20        21 Vss
```

I used a trailing "-" where the letters have a line over them in the published pinout. I got the info from pg 544 of "Programming the 65816 Including the 6502, 65C02, and 65802" by David Eyes and Ron Lichty, ABrady Book Published by Prentice Hall Press.

## //e, //c, Laser 128 Mouse pinouts

[Numbering is the same as the 9-pin game port connector.]



```
   Dsub-9 Female Socket on Computer    Dsub-9 Male Plug on Mouse
       ,--------------------.          ,--------------------.
      \  5   4   3   2   1  /          \  1   2   3   4   5  /
       \   9   8   7   6   /            \   6   7   8   9   /
        `-----------------'              `-----------------'

     Mouse          Usual //c, IIc+ Game Port Function

 1   MOUSE ID       Pushbutton 1
 2   +5V            +5V
 3   GND            GND
 4   XDIR           no Game Port function on //c, IIc+;
                    this TTL-compatible input can be read at $C066
 5   XMOVE          Game Control 0 or PDL0 (Joystick X-axis)
 6   n.c.           (no Game Port function on //c, IIc+)
 7   MOUSE BUTTON   Pushbutton 0
 8   YDIR           Game Control 1 or PDL1 (Joystick Y-axis)
 9   YMOVE          no Game Port function on //c, IIc+;
                    this TTL-compatible input can be read at $C067
```

## 3.5 in. and 5.25 in. Drive cable pinouts

Much of this information comes from page 90 of Open-Apple Volume 1, number 11 (1985).

The following table lists all of the drive control signals for each type of controller card/disk port. </pre>

| Signal Function | Unidisk | IIc | IIgs | Disk ][ |
|---|---|---|---|---|
| GND ground reference | 1-4 | 1-4 | 1-3 | 1,3,5,7 |
| -12V -12 volts DC | 5 | 5 | 5 | 9 |
| +5V +5 volts DC | 6,16 | 6 | 6 | 11,12 |
| +12V +12 volts DC | 7,8 | 7,8 | 7,8 | 13,15,17,19 |
| WRPROT write protect | 10 | 10 | 10 | 20 |
| PH 0-3 stepper motor phases | 11-14 | 11-14 | 11-14 | 2,4,6,8 |
| WREQ write request | 15 | 15 | 15 | 10 |
| DRVEN drive enable | 17 (9) | 17 | 17 (9) | 14 |
| RDDATA read data | 18 | 18 | 18 | 16 |
| WRDATA write data | 19 | 19 | 19 | 18 |
| EXTINT external interrupt | - | 9 | - | - |
| 3.5DISK Apple 3.5 drive enable | - | - | 4 | - |
| HDSEL 3.5" drive head select | - | - | 16 | - |
| not connected | - | 16 | - | - |

The UniDisk uses pin 9 to select the second drive. Inside each UniDisk, the signal from pin 9 at the computer is connected to pin 17 of the daisy- chain drive connector. When the computer selects drive 2 by activating pin 9, the first drive passes this through and the second drive sees its enable signal on pin 17. Thus all drives are identical.

The Disk ][ controller has two drive connectors, and the same pin (14) is used on each connector to select the appropriate drive. This signal is the only difference between the connectors – all other signals are connected in parallel.

Despite the IIgs having special functions for pins 4 and 16, they may be ignored when dealing with 5.25" drives, and treated as a UniDisk controller (i.e. connect pin 4 to ground, and pin 16 to +5V). The Apple 3.5 drive disconnects these signals internally, so that they will not interfere with its operation.

The UniDisk, IIc external drive and equivalents use a DB-19 connector, in which the pins are numbered along

the connector, i.e.

```
,-----------------------------------------------.
\ 1    2    3    4    5    6    7    B    9    10 /
 \  11   12   13   14   15   16   17   18   19   /
  `-------------------------------------------'
```

The Disk ][ uses an IDC-20 (20 pin insulation displacement connector) in which the pins are numbered in columns, i.e.

```
+-------------------------------------------------+
| 2    4    6    8    10   12   14   16   18   20 |
| 1    3    5    7    9    11   13   15   17   19 |
+-------------------------------------------------+
```

The above numbering is from the back of the plug (where the ribbon cable connects to the plug).

```
If you are looking at the front of the plug (the  socket side), reverse the rows in t
```

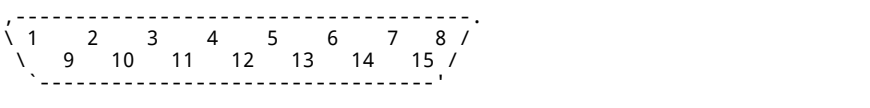
(top row is 1, 3, ...)

The pin numbering of the DB-19 connector does NOT correspond to the wire numbers in the cable. Pin 1 of the cable goes to pin 1 of the connector, but pin 2 of the cable goes to pin 11 of the connector.

## Apple DuoDisk 5.25 Cable Pinout

```
The diagram depicts the male end of the cable.

DB 19:

,-------------------------------------------------.
\ 01   02   03   04   05   06   07   0B   09   10 /
 \  11   12   13   14   15   16   17   18   19   /
  `-----------------------------------------------'


DB 25 looking at the end of the cable:  (x = no pin)

1, 13, 22 & 25 have no pin on some OEM cables, you may need to break out a pin or pul
the blocking plug out of the connector on the disk drive. This is to keep Apple paral
cables from being plugged into the drive. But you won't do that, will you? ;-)

,-------------------------------------------------.
\ 01  02  03  04  05  06  07  08  09  10  11  12  13 /
 \  14  15  16  17  18  19  20  21  22  23  24  25  /
  `-----------------------------------------------'

Cable

DB 19   DB 25

1       2
2       4
3       9  & 21
4       10 & 14
5       23
6       7
7       19
8       20
9       8
10      12
11      15
12      16
13      17
14      18
15      5
16      24
17      11
18      3
19      6
```

## Apple //c DA-15 Video Expansion Connector



```
1- TEXT Video text signal from TMG; set to inverse of GR, except in double high-resol
2- 14M 14M master timing signal from the system oscillator.
3- SYNC* Displays horizontal and vertical synchronization signal from IOU pin 39.
4- SEGB Displays vertical counter bit from IOU pin 4; in text mode, indicates second
    vertical counter; in graphics mode, indicates low-resolution.
5- 1VSOUND One-volt sound signal from pin 5 of the audio hybrid circuit (AUD).
6- LDPS* Video shift-register load enable from pin 12 of TMG.
7- WNDW* Active area display blanking; includes both horizontal and vertical blanking
8- +12V Regulated +12 volts DC; can drive 300mA.
9- PRAS* RAM row-address strobe from TMG pin 19.
10- GR Graphics mode enable from IOU pin 2.
11- SEROUT* Serialized character generator output from pin 1 of the 74LS166 shift reg
12- NTSC Composite NTSC video signal from VID hybrid chip.
13- GND Ground reference and supply.
14- VIDD7 From 74LS374 video latch; causes half-dot shift high.
15- CREF Color reference signal from TMG pin 3; 3.58 MHz.
```

Note. The signals at the DA-15 on the Apple IIc are not the same as those at the DA-15 end of the Apple III, Apple IIGS, and Macintosh II. Do not attempt to plug a cable intended for one into the other.

Several of these signals, such as the 14 MHz, must be buffered within about 4 inches of the back panel connector--preferably inside a container directly connected to the back panel.

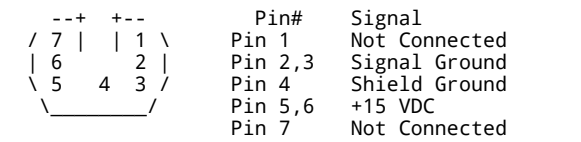
## Apple //c External Power Connector

From the Apple //c Technical Reference Manual

Section 11.2.2 The External Power Connector

The external power supply is attached to the internal converter by means of a 7-pin DIN connector. The connector pins are identified in Figure 11-1 and Table 11-3.

Figure 11-1 External Power Connector



```
    --+  +--          Pin#    Signal
  / 7 |  | 1 \      Pin 1     Not Connected
  | 6      2 |     Pin 2,3    Signal Ground
  \ 5   4  3 /     Pin 4      Shield Ground
   \________/      Pin 5,6    +15 VDC
                   Pin 7      Not Connected
```

Table 11-3 External Power Connector Signals

| Pin# | Name | Description |
|---|---|---|
| 1,7 | -- | Not Connected |
| 2,3 | Ground | Common Electrical Ground |
| 4 | Chassis | Chassis Ground |
| 5,6 | +15 | +15-volt DC input to converter |

## Apple //e Motherboard keyboard connector

From david@uow.edu.au (David E A Wilson)

Apple II Reference Manual For //e only [part # 030-0357-A spiral bound]

Understanding the Apple IIe by Jim Sather [Brady/Quality Software ISBN 0-8359-8019-7 ]

The latter is more useful as it gives you the matrix of switches as well.

```
J16 (Numeric Pad)         J17 (Keyboard)
11      X5                X6      26 25   Y7
10      X6                SHFT*   24 23   Y6
9       X4                Y9      22 21   X4
8       X7                X3      20 19   X5
7       n/c               X1      18 17   X7
6       Y5                X2      16 15   RESET*
5       Y2                XO      14 13   GND
4       Y4                Y8      12 11   CNTL*
3       Y3                Y5      10 9    CAPLOCK*
2       Y1                Y4      8  7    SW0/OAPL
1       Y0                Y3      6  5    SW1/CAPL
                          Y2      4  3    +5V
                          Y1      2  1    Y0

        Main Keyboard   Numeric Keypad
        XO      X1      X2      X3  |   X4      X5      X6      X7
------------------------------------+-------------------------------
YO      ESC     TAB     A       Z   |   /       )       *       ESC
                                    |
Y1      1!      Q       D       X   |   DOWN    UP      LEFT    RIGHT
                                    |
Y2      20      W       S       C   |   0       4       8       (
                                    |
Y3      34      E       H       V   |   1       5       9       -
                                    |
Y4      4$      R       F       S   |   2       6       .       RETURN
                                    |
Y5      6"      Y       G       N   |   3       7       +       ,
                                    +---------------------------------
Y6      5%      T       J       M       \|      `~      RETURN  DELETE

Y7      7&      U       K       ,<      +=       P      UP       DOWN

Y8      8*      I       ;:      .>      0)       [{     SPACE   LEFT

Y9      9(      O       L       /?      -_       ]}      '"      RIGHT
Notes:
1)      This is the US layout
2)      Early //e keyboard ROMs had ? LEFT ESC RIGHT SPACE replacing
        the ESC DOWN UP LEFT RIGHT in the numeric keypad section of the
        above diagram
3)      If you want more details such as the influence of the Control and
        CAPS LOCK keys or the DVORAK layout see pages 7-16 and 7-17
        of Jim Sather's Understanding the Apple IIe.
4)      Unlike the ][ & ][+, the //e keyboard is completely passive with
        the decoder chip located on the motherboard.
5)      The +5v connection is to run the power light and the Open/Closed
        Apple switches.
6)      The SHIFT, CONTROL, CAPSLOCK and RESET switches simply ground the
        appropriate pin of the connector (RESET via the CTRL line if the
        jumpers are in the standard setting).
```

## Apple //e Numeric Keypad connector

The pins are numbered from 1 to 11, with pin 1 being the closest to the keyboard end of the computer (as far as I can tell). The pin functions are:

1=YO, 2=Y1, 3=Y3, 4=Y4, 5=Y2, 6=Y5, 7=no connection, 8=X7, 9=X4, 10=X6, 11=X5.

The X/Y pins refer to keyboard X/Y matrix signals. Closing a specific X/Y pair is the equivalent of pressing the corresponding key on the keyboard.

The matrix is as follows.

```
   X7 X6 X5 X4
Y5  ,  +  7  3
Y4 CR  .  6  2
Y3  -  9  5  1
Y2  (  8  4  0
Y1                (see below)
YO     *  )  /
```

The YI row and YO/X7 intersection vary depending on which keyboard ROM you have.

The original IIe keyboard ROM (341-0132-B) has SPACE, RIGHT, ESC, LEFT, ?. I get the impression that this ROM is rare.

The revised IIe keyboard ROM (341-0132-C) has RIGHT, LEFT, UP, DOWN, ESC.

## Apple II/II+ Keyboard Socket

This socket is located near the front of the motherboard.

```
          +---| |----+
     +5v  | 1     16 | NC
  Strobe  | 2     15 | -12v
  ~Reset  | 3     14 | NC
      NC  | 4     13 | Data 1
  Data 5  | 5     12 | Data 0
  Data 4  | 6     11 | Data 3
  Data 6  | 7     10 | Data 2
     Gnd  | 8      9 | NC
          +----------+
```

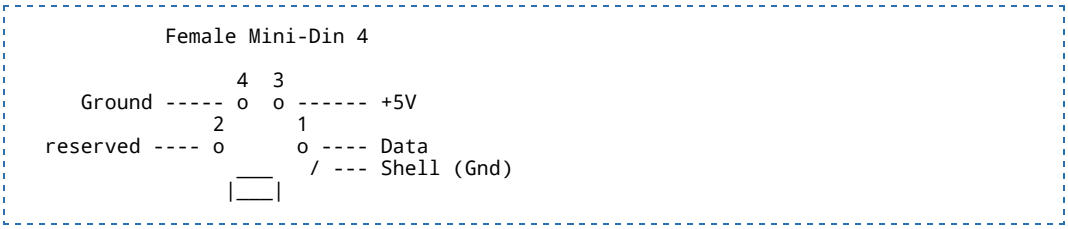
| Pin | Name | Description |
|---|---|---|
| 1 | +5 | +5 volt power supply. Total current drain on this pin must be less than 120mA. |
| 2 | STROBE | Strobe output from keyboard. This line should be given a pulse at least 10 microsecond long each time a key is pressed on the keyboard. The strobe can be of either polarity. |
| | ____ | ____ |
| 3 | RESET | Microprocessor's RESET line. Normally high, this line should be pulled low when the <RESET> key is pressed. |
| 4,9,16 | NC | No connection. |
| 5-7,10-13 | Data | Seven bit ASCII keyboard data input. |
| 8 Gnd | System electrical ground. | |
| 15 | -12v | -12 volt power supply. Keyboard should draw less than 50mA. |

## Parallel Printer DB-25 cable pinouts

... also the connections needed to connect that to a 'MPC parallel card'

```
MPC    DB25      Function
----   ----      --------------
1     17         Ground
2     10         ACK
6     15         Error
8      1         Strobe
9     12         Out of Paper
10     2         Data 0 (LSB)
11     3         Data 1
12     4         Data 2
13     5         Data 3
14     6         Data 4
15     7         Data 5
16     8         Data 6
17     9         Data 7 (MSB)
18    13         Select
20  19-25        Ground
```

# IIgs Apple Desktop Bus - ADB




Note: There is no connection on any IIgs to the "reserved" pin.